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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,675	06/18/2001	Youichi Ishimura	209544US2	7197

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EXAMINER
TRAN, THIEN F

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/881,675	Applicant(s) ISHIMURA ET AL.	
	Examiner Thien F Tran	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-5 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-5 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakurai et al. (US 5,962,877) in view of Sakurai et al. (JP 411284176A) and Okamoto et al. (US 4,903,117).

Sakurai et al. (US reference) discloses a field effect semiconductor device (Fig. 9b) having a semiconductor layer 2 of a first conductivity type (n-type), a collector region 1 of a second conductivity type (p-type) that is formed beneath said semiconductor layer and equipped with a collector electrode 13 on its lower surface, a base region 3 of the second conductivity type that is formed as part of the upper surface of said semiconductor layer, at least one pair of emitter regions 4 of the first conductivity type that are formed as part of the upper surface of said base region, an insulating layer 10 that is formed to contact said base region that is located between said emitter regions and said semiconductor layer, a gate electrode 11 that is placed on the upper surface of said insulating layer, an interlayer insulating film 14 that is formed to cover said gate

electrode, and an emitter electrode 12 that is formed over the interlayer insulating film, base region, and emitter regions. Sakurai et al. does not disclose a barrier metal layer formed to continuously contact said interlayer insulating film, base region, emitter regions, and under said emitter electrode. Sakurai et al. (Japanese reference) discloses a field effect semiconductor device (Fig. 2) comprising a barrier metal layer 21 of molybdenum silicide with a thickness of more than 60 nm formed to continuously contact an interlayer insulating film 12, base region 2, emitter regions 3, and under an emitter electrode 20 of aluminum. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to form the emitter electrode 12 of aluminum and provide a barrier metal layer having a thickness of more than 60 nm into the Sakurai et al.'s structure (US reference) as taught by the Japanese reference so that the barrier metal layer continuously contacts said interlayer insulating film, base region, and emitter regions in order to eliminate silicon residue and prevent aluminum diffusion into the silicon substrate. The modified Sakurai et al. does not disclose the barrier metal layer formed of titanium nitride. Molybdenum silicide and titanium nitride are barrier materials known in the art and routinely used to form barrier metal layer in semiconductor device as shown for example by Okamoto et al. (see Fig. 1 and col. 3, lines 3-15) to prevent spiking in the junction between the emitter electrode and the silicon substrate, to obtain low resistance ohmic contact and to serve as an excellent diffusion barrier between aluminum and silicon. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select either one of these materials as a suitable barrier material for the barrier metal layer of the

modified Sakurai et al., since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of design choice. In re Leshin, 125 USPQ 416.

Regarding claim 3, Sakurai et al. (Japanese reference) teaches the thickness of the barrier metal layer is 60 nm.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakurai et al. (US 5,962,877) in view of Sakurai et al. (JP 411284176A) and Okamoto et al. (US 4,903,117) as applied to claims 1-3 and 5 above, and further in view of Kim et al. (US 6,229,166).

The modified Sakurai et al. does not explicitly disclose the interlayer insulating film 14 having an impurity density less than 5 mol %. Undoped silicon oxide and impurity doped silicon oxide are dielectric materials known in the art and routinely used to form interlayer insulating film in semiconductor device as shown for example by Kim et al. (interlayer insulating film 108, col. 4, lines 7-12). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select either one of these materials as a suitable dielectric material for the interlayer insulating film 14 of the modified Sakurai et al., since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of design choice. In re Leshin, 125 USPQ 416. Since the layer 14 is undoped silicon oxide, the impurity density of the interlayer insulating film 14 is less than 5 mol %.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F Tran whose telephone number is (703) 308-4108. The examiner can normally be reached on 7:00AM - 3:30PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

tt
April 4, 2002

Thien Tran
Patent Examiner
Technology Center 2800